ABSTRACT

A high speed communications interface divides data into a plurality of lanes, each lane encoded with clocking information, serialized, and sent to an interface. During cycles when there is no available data to send, IDLE_EVEN and IDLE_ODD cells are sent on alternating cycles. Data is transmitted by sending a header which spans all lanes and includes a START symbol. The final data transaction includes a Frame Check Sequence (FCS) which operates over the entire header and data. The packet is terminated by an END symbol, which is sent after the final data, and the remainder of the lanes are padded with IDLE_EVEN, IDLE_ODD, IDLE_EVEN_BUSY, or IDLE_ODD_BUSY cycles. The interface has a variable clock rate.